THE COUNCIL OF COMMUNITY COLLEGES OF JAMAICA

ASSOCIATE OF SCIENCE EXAMINATION

SEMESTER II – 2019 MAY

PROGRAMME:	**ENGINEERING**
COURSE NAME:	**INTRODUCTION TO ELECTRONIC DEVICES AND CIRCUITS**
CODE:	**ELEC2409**
YEAR GROUP:	**TWO**
DATE:	**WEDNESDAY, 2019 MAY 8**
TIME:	**9:00 A.M. – 11:00 A.M.**
DURATION:	**2 HOURS**
EXAMINATION TYPE:	**FINAL**

This Examination Paper has **6** *Pages*

INSTRUCTION:

1. **THIS PAPER CONSISTS OF SIX (6) QUESTIONS. ANSWER ANY <u>FOUR (4)</u>**

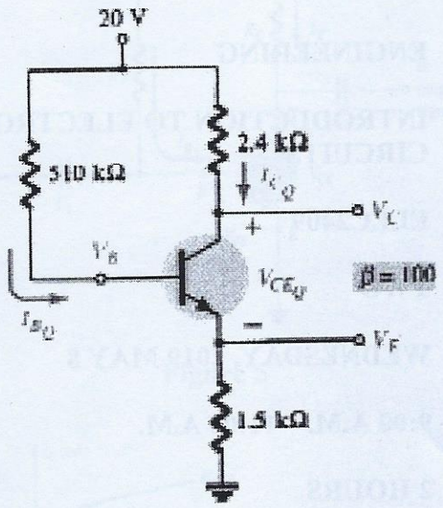
<u>DO NOT TURN THIS PAGE UNTIL YOU ARE TOLD TO DO SO</u>

Instruction: In the booklet provided, answer any <u>FOUR (4)</u> questions.

<u>Question 1</u>

A. Sketch the biasing diagrams and circuit symbols for the NPN and PNP transistors with a Common Base Configuration. ***(6 marks)***

B. For the emitter-stabilized bias circuit below, $V_{cc} = 20V$, $R_B = 510k\Omega$, $R_c = 2.4k\Omega$ and $R_E = 1.5k\Omega$ with $\beta = 100$.



Determine:

i. I_{Bq}
ii. I_{Cq}
iii. V_{CEq}
iv. V_C
v. V_E
vi. V_B
vii. V_{BC}

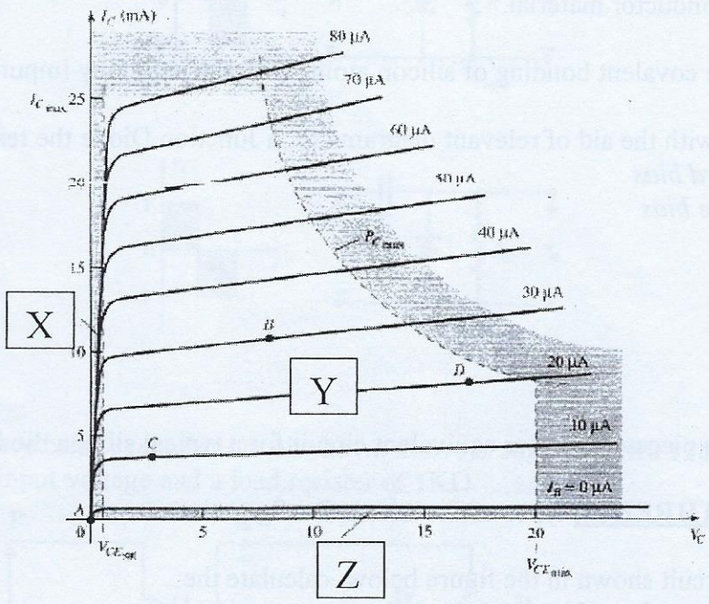
(14 marks)

(Total 20 marks)

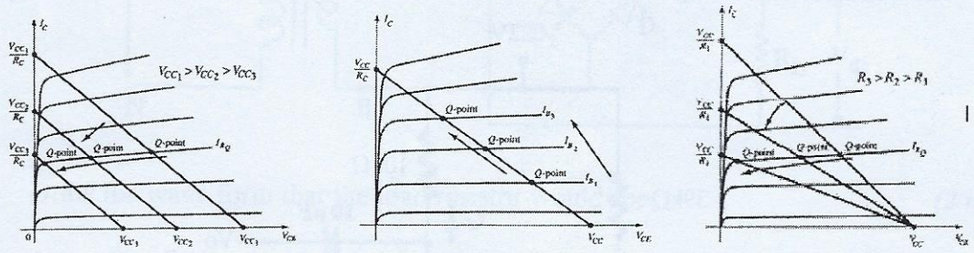
Question 2

A. State the name of the re-joins X, Y & Z in the figure below. ***(3 marks)***

B. Briefly explain the design properties for biasing a transistor at the following Q points (A, B, C, D) in the figure below. ***(8 marks)***



C. Describe the conditions that will result in the following Q point variations below.



(9 marks)

(Total 20 marks)

Question 3

A. Explain the difference between Intrinsic and Extrinsic semiconductor materials. *(4 marks)*

B.
i. What are the majority carriers of an **n-Type** and **p-Type** semiconductors? *(1 mark)*
ii. List **TWO (2)** elements that constitute the doping process of an **n-Type** semiconductor material. *(1 mark)*

C. Sketch the covalent bonding of silicon atoms with the antimony impurity atom. *(4 marks)*

D. Describe with the aid of relevant diagrams for a Junction Diode the terms:
i. *forward bias*
ii. *reverse bias* *(10 marks)*

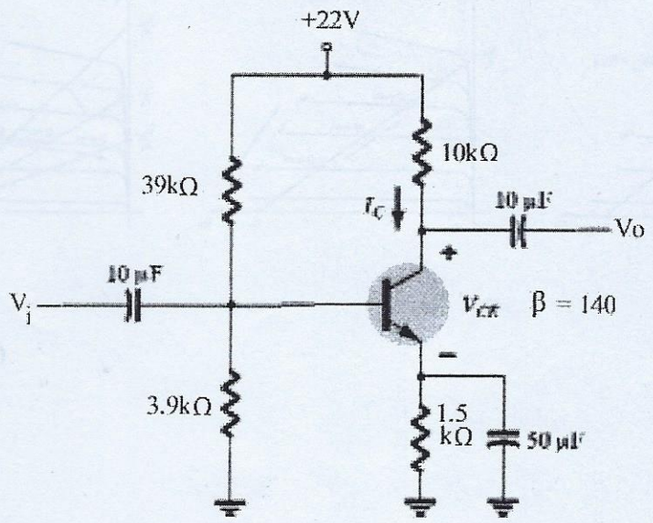
(Total 20 marks)

QUESTION 5

A. Sketch the piecewise-linear equivalent circuit for a typical silicon diode. *(5 marks)*

B. State the **THREE (3)** types of Transistor Configurations. *(3 marks)*

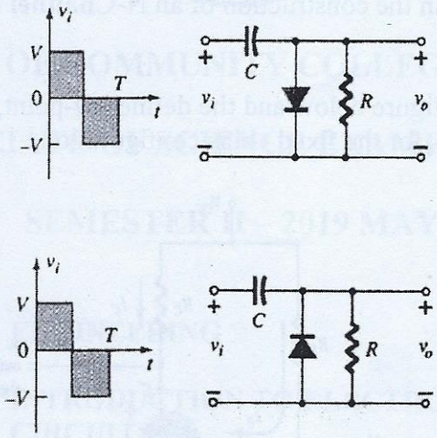
C. For the circuit shown in the figure below, calculate the:
i. DC bias voltage $\mathbf{V_{CE}}$
ii. base current $\mathbf{I_B}$
iii. collector current $\mathbf{I_C}$ *(12 marks)*



(Total 20 marks)

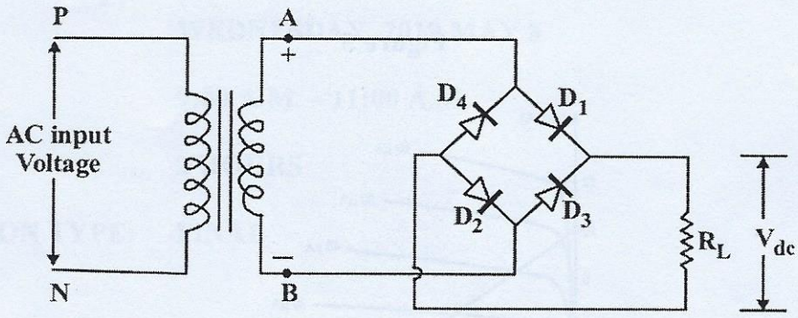
Question 4

A. Draw the output waveform, V_o, for the clamping network for the square wave with a max. input of 60 V.



(6 marks)

B. The full-wave bridge rectifier circuit shown above is supplied with *118.43* peak sinusoidal input voltage and a load resister of 1KΩ



i. Draw the wave form that the load resistor would see. *(2 marks)*

ii. Assuming diodes are ideal, what is the dc voltage available at the load resistor? *(4 marks)*

iii. If silicon diodes are employed, what is the dc voltage available at the load? *(3 marks)*

iv. Determine the required PIV rating for each Si diode. *(2 marks)*

v. Find the max current through each diode during conduction. *(3 marks)*

(Total 20 marks)

Question 6

A. Explain the terms **N-Channel** and **P-Channel** field effect transistors. ***(4 marks)***

B. Use a diagram to explain the construction of an **N-Channel** field effect transistor. ***(8 marks)***

C. Given the load line of Figure below and the defined Q-point, determine the required values of V_{cc}, R_c and R_b for the fixed –bias configuration.

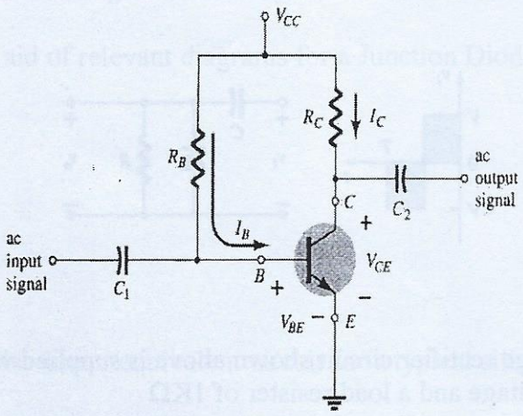


Figure 5

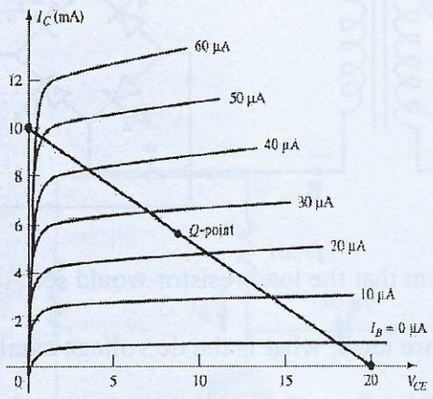


Figure 6

(8 marks)

(Total 20 marks)

END OF EXAMINATION